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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,852	10/22/2001	Ko-Yan Shih	JCLA7022	9319

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,852	SHIH ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *2,5,6,8,10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Priority

The examiner acknowledges the applicant's claim for priority under 35 USC 119.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the "Select" line label as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

1. The disclosure is objected to because of the following informalities: page 4 line 9 repeats the phrase "has to be". Appropriate correction is required.

Claim Objections

2. Claim 2 is objected to because of the following informalities: line 16 of page 11 recites "the next state" but has no true antecedent. The examiner requests that the

applicant change the phrase to "a next state", in accordance with a similar phrase on page 12 line 14. Appropriate correction is required.

3. Claims 2, 5, 6, 8 and 10 are objected to because of the following informalities: the claims have the word "multiplexing" misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The preamble of the claim is indefinite in that "the circuit comprising" may be interpreted as being either of the two preceding circuits. The examiner requests that the applicant be more specific as to which circuit is meant to be further limited.

6. Claim 2 recites the limitation "the test activating signal" in page 11 line 17. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 6 recites the limitation "the test results" in page 12 line 16. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 8 recites the limitation "the test results" in page 11 line 22. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Iknaian et al., U.S. Patent No. 5198758. Iknaian et al. teaches a method of testing a chip that comprises an intellectual product circuit module (see Abstract and column 8 lines 65-68) which in the reference is a delay regulator circuit, the method comprising: providing a test pattern (column 9 lines 10-14); configuring a plurality of registers (FIG.6 61 and column 10 lines 20-23) in a plurality of different states according to the test pattern (column 9 lines 110-16 and column 5 lines 33-63); and providing a test activating signal to the intellectual product circuit module (column 9 lines 21-23) in a next state (column 9 lines 33-63), so that the intellectual product circuit module operates according to the test pattern (column 9 lines 24-29).

10. Claims 2-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al., U.S. Patent No. 5592493.

As per Claim 2:

Crouch et al. teaches a circuit for testing a chip (see Abstract) that comprises an intellectual product circuit module (FIG.1 12, 14, 16, 18, 20, 22), the circuit comprising: a plurality of registers (for example: FIG.2 70-84), coupled to the intellectual product circuit module to output signals stored in the registers to the intellectual product circuit module (FIG.2 66); and a multiplexing finite state machine

controller (FIG.2 10), coupled to the intellectual product circuit module and the registers (see FIG.1), wherein the multiplexing finite state machine controller receives a test pattern (column 6 lines 1-9) and configures the registers in a plurality of different states, in the next state the multiplexing finite state machine controller further provides the test activating signal to the intellectual product circuit module (column 6 lines 9-22) so that the intellectual product circuit module is operated and tested according to outputs of the registers (example: column 6 lines 23-30).

As per Claim 3:

Crouch et al. teaches the circuit according to claim 2, wherein the intellectual product circuit module further comprises a plurality of ports coupled to the registers (example: FIG.2. 77 and 76 to 66).

As per Claim 4:

Crouch et al. teaches the circuit according to claim 2, wherein the test activating signal includes a synchronous clock signal (FIG.1 PCLK and column 6 line 25).

As per Claim 5:

Crouch et al. teaches the circuit according to claim 2, wherein each of the registers further comprises an enable input terminal (FIG.1 MTM, TSTADDR, S_SE, STDI) coupled to the multiplexing finite state controller capable of controlling the registers and asserting an enable signal to enable the registers to buffer the test pattern (column 7 lines 54-67 and column 8 lines 1-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claim 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crouch et al., U.S. Patent No. 5592493, and further in view of Shacham et al., U.S. Patent No. 6493840.

As per Claim 6:

Crouch et al. teaches a circuit for testing a chip that comprises a plurality of intellectual product circuit modules (FIG.1 12, 14, 16, 18, 20, 22), comprising: a plurality of registers (for example: FIG.2 70-84), coupled to the intellectual product circuit modules to output signals stored in the registers to the intellectual product circuit modules (FIG.2 66); and a multiplexing finite state machine controller (FIG.2 10), coupled to the intellectual product circuit modules, the multiplexer controller and the registers (see FIG.1), the multiplexing finite state machine controller receiving a test pattern (column 6 lines 1-9) to configure the registers in a plurality of different states, and providing a test activating signal to one of the intellectual product circuit modules in a next state, so that the intellectual product circuit module is operated according to the output of the registers (example: column 6 lines 23-30), and the multiplexing finite state machine controller further controlling a multiplexer controller (FIG.2 10 MUX) to selectively output the test results (FIG.2 SCAN DATA OUT). However, Crouch et al. fails to teach a multiplexer controller, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules. In an analogous art, Shacham et al., in FIG.2 teaches a multiplexer controller (FIG.2 1), coupled to the intellectual product circuit modules (FIG.2 1) to selectively output a test result from the intellectual product circuit modules (FIG.2 44). It would have been

obvious to modify the circuit of Crouch et al. by adding the multiplexer as taught by Shacham et al. in order to select test outputs. And Shacham et al., in column 1 lines 50-65, boasts of an advantage being a less costly way to provide test coverage for circuits through the manufacturing stages. One with ordinary skill in the art at the time of the invention, motivated by Shacham et al., would combine the art, and so the claim is rejected.

As per Claim 7:

Crouch et al. further teaches the circuit according to claim 6, wherein each of the intellectual product circuit modules comprises a plurality of ports coupled to the registers (example: FIG.2. 77 and 76 to 66).

As per Claim 8:

Crouch et al. further teaches the circuit according to claim 6, wherein the multiplexer controller further comprises a select input terminal coupled to the multiplexing finite state machine controller (FIG.1 TSTADDR), so that the multiplexing finite state machine controller controls the multiplexer controller to selectively output the test result (FIG.2 10 and SCAN DATA OUT).

As per Claim 9:

Crouch et al. further teaches the circuit according to claim 6, wherein the test-activating signal comprises a synchronous clock signal (FIG.1 PCLK and column 6 line 25).

As per Claim 10:

Crouch et al. further teaches the circuit according to claim 6, wherein each of the registers further comprises an enable input terminal (FIG.1 MTM, TSTADDR, S_SE, STDI) coupled to the multiplexing finite state machine controller, which respectively controls and enables the registers to buffer the test pattern (column 7 lines 54-67 and column 8 lines 1-26).

As per Claim 11:

Crouch et al. further teaches the circuit according to claim 6, wherein the chip is a system on chip (column 1 lines 5-30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

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